AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1-12. **(Canceled)**

13. **(Previously Presented)** An integrated circuit for use in a transceiver module, the integrated circuit comprising:

a first electrical input port for receiving a first serial electrical data stream;

receiver eye opener circuitry including components for retiming and reshaping the first serial electrical data stream, the components including a clock and data recovery, an equalizer, and a coefficient module, wherein the equalizer used a clock from the clock and data recovery and coefficients generated by the coefficient module to condition the first serial electrical data stream;

a first electrical output port for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit;

a second electrical input port for receiving a second serial electrical data stream from external to the integrated circuit;

transmitter eye opener circuitry including components for retiming and reshaping the second serial electrical data stream;

a second electrical output port for transmitting the retimed and reshaped second serial electrical data stream; and

a bit error rate tester (BERT) engine for testing a test data path from a starting test point to an ending test point, the starting test point and the ending test point each located on either a receive path or on a transmit path, wherein the receive path is from the first electrical input port through the receiver eye opener circuitry to the first electrical output port and the transmit path is from the second electrical input port through the transmitter eye opener circuitry to the second electrical output port.

14. **(Original)** The integrated circuit of claim 13 wherein the test data path includes the retiming and reshaping components of the receiver eye opener circuitry.

15. **(Original)** The integrated circuit of claim 13 wherein the test data path includes the retiming and reshaping components of the transmitter eye opener circuitry.

16. **(Original)** The integrated circuit of claim 13 wherein the test data path includes the second electrical output port and the first electrical input port.

17. **(Original)** The integrated circuit of claim 16 wherein:

the starting test point is located between the retiming and reshaping components of the transmitter eye opener circuitry and the second electrical output port; and

the ending test point is located between the first electrical input port and the retiming and reshaping components of the receiver eye opener circuitry.

18. **(Original)** The integrated circuit of claim 13 wherein each of the starting test point and the ending test point is located between the first electrical input port and the retiming and reshaping components pf the receiver eye opener circuitry, between the retiming and reshaping components of the receiver eye opener circuitry and the first electrical output port, between the second electrical input port and the retiming and reshaping components of the transmitter eye opener circuitry, or between the retiming and reshaping components of the transmitter eye opener circuitry and the second electrical output port.

19. **(Original)** The integrated circuit of claim 13 wherein the BERT engine generates a test pattern at a data rate of at least approximately 10 Gb/s.

20. **(Original)** The integrated circuit of claim 13 wherein the BERT engine comprises:

pattern generator circuitry coupled to the starting test point, for generating a test pattern for testing the test data path; and

error detector circuitry coupled to the ending test point, for detecting errors in the test pattern.

21. **(Original)** The integrated circuit of claim 13 further comprising:

BERT control circuitry coupled to the BERT engine for controlling testing of the test data path.

22. **(Original)** The integrated circuit of claim 13 further comprising:

power management circuitry for powering down the BERT engine when no testing of the test data path is occurring.

23. **(Canceled)**

24. **(Canceled)**

25. **(Canceled)**

26. **(Previously Presented)** An integrated circuit for use in a transceiver module, the integrated circuit comprising:

first input means for receiving a first serial electrical data stream;

first eye opener means for retiming and reshaping the first electrical data stream;

first output means for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit;

second input means for receiving a second serial electrical data stream from external to the integrated circuit;

second eye opener means for retiming and reshaping the second serial electrical data stream, wherein the second eye opener means further conditions the second serial electrical signal using an equalizer and a clock and data recovery;

second output means for transmitting the retimed and reshaped second serial electrical data stream; and

BERT testing means for testing a test data path from a starting test point to an ending test point, the starting test point and the ending test point each located on either a receive path or on a transmit path, wherein the receive path is from the first input means through the first eye opener means to the first output means and the transmit path is from the second input means through the second eye opener means to the second output means.